**Seizing the Semiconductor Opportunity**

**How California can Increase its Competitiveness and Capture CHIPS Act Funding**

**The CHIPS Act: What it Does**

The Creating Helpful Incentives to Produce Semiconductors and Science Act of 2022 (CHIPS+Science Act) signed into law on August 9, 2022. The product of parallel bills in the House and Senate – America COMPETES in the House and USICA (the United States Innovation and Competition Act) in the Senate. While many other provisions were stripped out, funding for semiconductor manufacturing and research was at the core of both the House and Senate versions and of the final bill, reflecting bipartisan agreement on the importance of semiconductors to the economy and national security, and on the need to increase semiconductor manufacturing in the United States. In addition to its provisions on semiconductor, the Act more broadly invests in scientific research, the commercialization of leading-edge technologies, and the STEM workforce, and establishes new regional technology and innovation hubs to increase opportunity in regions of the United States outside historic technology centers.

Breaking this down specifically, the Act contains $278 billion in new funding:

* $200 billion is authorized for scientific R&D, and workforce and economic development programs at the National Science Foundation ($81B), the Department of Energy ($67.1B), the Economic Development Administration ($11B), the Department of Commerce ($10B), and NASA.
* $3 billion targets programs focused on leading edge technology and wireless supply chains.
* $52.7 billion is appropriated for semiconductor manufacturing, R&D and workforce development, with another $24 billion in tax credits allocated for chip production.

The distinction between authorization and appropriation is key. Only funds for semiconductor development have been appropriated and are currently available to be committed. The balance of funding, primarily for science, is only authorized and still must go through the appropriations process.

Of the funds allocated to *semiconductors*, $52.7 billion will be invested over five years to support domestic manufacturing, including $39 billion in manufacturing incentives ($6 billion will provide loans and loan guarantees to support a $75 billion direct loan and loan guarantee program) and $13.2 billion to support R&D and workforce development.[[1]](#footnote-1)

Within those figures, in the national security and defense field $2 billion is allocated to the Department of Defense to fund microelectronics research, fabrication and workforce training (the CHIPS for America Defense Fund), $500 million to the Department of State to coordinate with overseas government partners on semiconductor supply chain security (the CHIPS for America International Technology Security Fund), $2 billion for the National Semiconductor Technology Center, $2 billion to the National Advance Packaging Manufacturing Program, $500 million for Manufacturing USA Institutes, $6 billion to National Institute of Standards and Technology (NIST) for semiconductor programs, $200 million to the CHIPS for America Workforce and Education Fund, and $1.5 billion to the Public Wireless Supply Chain Innovation Fund to support hardware and software supply chains for 5G networks open radio access (ORAN) networks.

In addition to direct funding, private entities are eligible for a 25% advanced manufacturing investment tax credit for investments in semiconductor manufacturing and related processing equipment – an amount that the Congressional Budget Office (CBO) expects will generate $24 billion in activity over the next five years.

**Why Semiconductor Investment is Important**

Semiconductor companies fall into three main baskets: integrated device manufacturers (IDMs), fabless, and foundries. *Integrated Device Manufacturers* handle the complete manufacturing process from design through production, *Fabless* companies design semiconductors but outsource their production. The outsourced production of semiconductors is done by *foundries*. Major IDMs in the United States include Intel, Micron, and Texas Instruments. Fabless companies include Qualcomm, Nvidia, Broadcom, AMD and Marvell, all based in California. Other industry leaders including Samsung, TSMC, Texas Instruments and Global Foundries also have a presence. In addition to companies that produce semiconductors, the industry includes companies that produce the tools and equipment to manufacture semiconductors. Industry leaders in this segment include. Industry leaders in this segment include ASML, KLA Tencor, Lam Research, and Applied Materials.

Passage of the bill stemmed from the recognition that where the United States produced 37% of the world’s semiconductor chips in the 1990s it produces only 12% today, and none of the most advanced chips. Seventy-five percent of chips consumed in the United States are now produced in East Asia. This happened as production moved offshore to countries with lower costs and particularly to Taiwan, where TSMC is now the world’s leading produced of advanced chips. Looking beyond the United States’ acknowledged leadership in research and design, the ubiquity of chips in modern technology, US-China tensions, and the potential vulnerability of shipments from Taiwan have together increased the focus on manufacturing and the need to develop a more integrated capacity. Chip shortages in 2021 reportedly cost the U.S. economy $240 billion, particularly affecting the automotive sector.[[2]](#footnote-2)

In addition to supporting national security goals and economic competitiveness, new investment in chip manufacturing is expected to bring major economic benefits to the regions where it occurs. In 2021 the Semiconductor Industry Association estimated that $50 billion in federal incentives would directly create 43,000 in new semiconductor industry jobs, and a total of 280,000 permanent jobs when the secondary effects of increased semiconductor manufacturing are included. 185,000 temporary jobs would also be created as new fabs are constructed, adding close to $25 billion to the economy. The industry, with a total economic impact of $246.4 billion in 2020, currently employs more than 277,000 workers in high-paying jobs in R&D, design and manufacturing, and supports 1.6 million additional jobs indirectly. The secondary employment impacts are attributable to the industry’s high jobs multiplier factor of 6.7, meaning that for each worker directly employed in the semiconductor sector an additional 5.7 jobs are supported in the wider economy. One in five workers in the industry has not attended college, indicating that the semiconductor sector is a significant source of blue-collar opportunities. It also employs a larger share of non-white workers than the national average for industry.[[3]](#footnote-3)

**Semiconductor Inductor Industry Employment by State**

Rank State Employment % US Rank State Employment %US

1 California 63,300 23% 7 Massachusetts 12,200 4%

2 Texas 43,800 16% 8 New York 10,200 4%

3 Oregon 40,300 15% 9 North Carolina 7,900 3%

4 Arizona 28,900 10% 10 Washington 5,000 2%

5 Florida 12,900 5% 11 Virginia 4,100 1%

6 Idaho 12,300 4% 12 Ohio 4,000 1%

Source: Semiconductor Industry Association

**The Competitive Landscape**

In competing for CHIPS funds California is entering an already competitive landscape.

In the run-up to the Act’s passage industry investors communicated to federal officials that with investment decisions pending and the high cost of production in the United States, decisions on where to manufacture would be influenced by the passage of the bill, as subsidies were considered to narrowing the 35-45% cost gap between producing chips domestically and overseas. In its aftermath, **Micron** announced an initial $20 billion investment in upstate New York, a figure that could rise over time to $100 billion. In addition to federal support the package of incentives included $5.5 billion in incentives from the State of New York. That followed a July announcement that the company would invest $15 billion in a new factory in Idaho.[[4]](#footnote-4)

Also in August, **Qualcomm** and **GlobalFoundries** announced a new partnership that includes a $4.2 billion purchase agreement to buy chips produced through an expansion of GlobalFoundries’ facility in upstate New York, adding to a $3.2 billion purchase agreement that was announced earlier.[[5]](#footnote-5) Qualcomm, a fabless semiconductor company, says it will increase production in the U.S. by up to 50% over the next five years.

**Intel**, which plans to build a massive semiconductor plant in Ohio, also indicated that the pace of its development would depend on the passage of CHIPS. To secure the investment the State of Ohio offered Intel $1.9 billion in cash, infrastructure improvements, and tax breaks plus $150 million from JobsOhio and local property tax abatements. To secure the site the city of New Albany annexed 1,689 acres of Jersey Township, providing 900 acres for Intel, rezoning the land from Agricultural to the new classification Technology Manufacturing District. Other locational benefits that Intel found to be beneficial included land availability, affordable utilities, an ample water supply (though some may be recycled semiconductor fabs can use 5 million gallons of water a day), and proximity to universities, ports and airports.[[6]](#footnote-6)

Overseas companies are also actively expanding production in the U.S. Taiwan’s **TSMC** has committed to investing $12 billion in a fab in Arizona that will produce chips by 2024. Korea’s **Samsung** is building an advanced production facility in Taylor, Texas with a $17 billion investment and has announced plans for 11 additional fabs by at its complexes in both Taylor and Austin.

Noteworthy in all these projects is the level of direct subsidy provided by state and local governments.

Among the leading states competing for CHIPS funding Arizona is out in front with the launch of a National Semiconductor Economic Roadmap. Texas has launched a National Semiconductor Centers Texas Task Force to secure NSTC and advanced packaging R&D. New York, working with the State University of New York (SUNY) is aggressive at both the state and local levels. Oregon is behind other states but is mobilizing.

**Implementing the CHIPS Act**

Sections 9902 and 9906 of the National Defense Authorization Act of 2021 (NDAA) authorized a range of semiconductor related manufacturing and R&D activity, including the funding of applicants to incentivize investment in facilities and equipment for the fabrication, assembly, testing, packaging, or R&D of semiconductors or semiconductor manufacturing equipment. This can happen through grants, cooperative agreements, loans, and loan guarantees. The CHIPS Act appropriates $39 billion for these purposes, to be distributed through the Department of Commerce.

NDAA also authorizes the Department of Commerce to establish a *National Semiconductor Technology Center* (NSTC) to conduct research and prototyping of or the prototyping of advanced semiconductor technology, and the establishment of a *National Advanced Packaging Manufacturing Program* (NAPMP) led by NIST (the National Institute of Standards and Technology). It also authorizes NIST to establish up to three *Manufacturing USA* institutes to advance research and commercialization of semiconductor manufacturing technologies and carry out R&D to advance measurement science, standards, material characterization, instrumentation, testing and manufacturing. The CHIPS appropriates $11 billion for these purposes. Both sections of the NDAA authorize and direct investments in the semiconductor workforce.

In addition to appropriating resources to fund provisions of the NDAA, the CHIPS Act creates a new advanced manufacturing investment tax credit equal to 25% of the value of qualified investments in buildings and depreciable property with the primary purpose of manufacturing semiconductors or semiconductor manufacturing equipment, to be administered by the Internal Revenue Service. The credit is available for projects that start construction between January 1, 2023 and December 31, 2026.

The Department of Commerce intends to implement the CHIPS Act through two new offices housed at NIST: the **CHIPS Program Office** (CPO) and the CHIPS R&D Office. The CPO will be responsible for the implementation of incentive programs and will coordinate all CHIPS related activity in the Department of Commerce and across government agencies. The **CHIPS R&D Office** will incubate the NSTC and manage R&D activity and the Advanced Packaging and Manufacturing USA programs.

Applicants for funding can be a private entity, non-profit, consortium of private entities, or consortium of non-profit, public and private entities. CHIPS funds, for which both domestic and foreign companies are eligible, must be used for facilities built in the United States. Applicants are encouraged to consider collaborations with suppliers, customers, state and local governments, and other relevant entities.

The Commerce Department’s activity will be bundled into three initiatives, each with different strategic imperatives and time horizons but potentially overlapping stakeholders:

**Large-scale Investments in leading-edge logic and memory manufacturing clusters:** The Department will invite proposals for the construction or expansion of manufacturing facilities the fabrication, packaging, assembly and testing of leading-edge logic and memory chips. Funding may be provided through grants, subsidized loans or loan guarantees. Solicitation of proposals will begin within six months of enactment of the CHIPS Act (February 2023). This activity is expected to account for the largest part of CHIPS Act funding - $28 billion.

**Expanding manufacturing capacity for mature and current-generation chips, new and specialty technologies, and for suppliers to the industry**: The goal here is to increase domestic production across a spectrum, including chips used in defense and in commercial sectors such as automobiles, ICT and medical devices. Industry participants are invited to craft creative proposals. This could include the construction or expansion of facilities for the production of current generation and legacy chips, facilities for the production of new or specialty technologies, facilities that manufacture equipment and materials for semiconductor manufacturing, potentially co-located in regional clusters, and equipment upgrades that provide near-term efficiency improvements in fabs. Funding may be available through grants, loans or loan guarantees. Solicitation of proposals will begin within six months of the CHIPS Act entering into force (February 2023). Approximately $10 billion is expected to be committed in this area.

**Initiatives to strengthen U.S. leadership in R&D:** R&D initiatives, covering the NSTC (National Semiconductor Technology Center), NASPMP, the manufacturing USA Institutes, and NIST metrology investments, will receive $11 billion in CHIPS Act funding and are expected to operate in coordination with each other, with the incentives program, and with microelectronics R&D programs supported by other U.S. Federal agencies.

* **National Semiconductor Technology Center (NSTC):** The NSCT will be a public-private entity that includes participation from industry, universities, the Departments of Defense and Energy, and the National Science Foundation (NSF), Funding provided through the CHIPS Act is seen as seed capital for what eventually will be a larger organization driving innovation in semiconductors and microelectronics with financial and programmatic support form universities, investors and other government agencies including those at the state and local levels. Collaborators and research partners from around the world, and particularly from allied countries, will be welcome. Research is expected to focus on advanced semiconductor design, scaling new manufacturing processes, developing new tools and materials, improving the lab-to-fab flow, and standards and technical roadmaps. The NSCT will also address workforce development and the pipeline of workers needed to support an expanding sector. It is expected to play a key role in coordinating and scaling up programs currently led by industry associations, private companies, state and local governments, and other federal agencies. The CHIPS R&D Office will incubate the NSTC.
* **National Advanced Packaging Manufacturing Program (NAPMP)**: Fabricated semiconductors are “packaged” in a container that attaches to printed circuit boards that eventually appear in products. Most packaging is labor-intensive, is done in Asia, and will be economically difficult to bring home. The United States can compete, however, in advanced packaging, which is expected to account for 50% of packaging revenue by 2024. Innovations in advanced packaging are increasingly being integrated into the semiconductor process flow, blurring the distinction between silicon and packaging. NAPMP, which will operate under NIST, will foster a network of related entities in the field, and work with network participants to establish a pilot packaging facility to enable the testing and integration of new processes.
* **Manufacturing USA Institute**: 16 Manufacturing Institutes currently exist, engaging government, manufacturing and academic organizations, with the goal of training the manufacturing workforce and driving new products to market. NIST will establish up to three new Manufacturing USA Institutes to bring together industry and university partners to focus on semiconductor manufacturing challenges. Virtualization of wafer production processes and the improved of automation process and materials handling will be key topics.
* **Metrology Research**: Measuring semiconductors throughout the fabrication process is essential to fabrication, with exacting requirements for materials purity, defect tolerances, materials properties, and in-line processes. NIST plans to expand ongoing metrology research programs in measurement to enable breakthrough, standards and process capability.

Taken together, these initiatives are intended to create robust networks for innovation within the U.S. semiconductor ecosystem. Since the current cost of building a fab can exceed $10 billion, the $50 billion available through the CHIPS Act is insufficient by itself to fund large-scale expansions to the system, and development of a small number of new domestic fabs by itself won’t fundamentally impact U.S. competitiveness or supply chain security. Instead, funds available through the Act must leverage private sector and other investment in order to catalyze a larger and deeper semiconductor sector.

In other criteria that will influence awards, CPO will:

* implement a Congressional-mandated requirement that any company that receives funding be prohibited for ten years from engaging in significant transactions involving the material expansion of semiconductor manufacturing in China.
* prioritize applicants with proposals designed to increase participation by economically disadvantaged individuals, minority-owned businesses, women-owned businesses, and rural businesses.
* encourage large-scale investments that can attract associated suppliers and workforce investment, and proposals that leverage private capital.
* encourage collaborations, including consortium-like proposals, among fabricators and their upstream suppliers, equipment providers, and downstream partners.
* prioritize projects that include state and local incentives such as workforce investment and long-term tax credits.
* Encourage projects that include workforce development at a scale required to meet demand. This includes programs that enable employers, training providers, workforce development organizations, labor unions, and other stakeholders work together to create more paid training and experiential apprenticeship programs for skills development.

Finally, and this is key for California, the Department of Commerce will prioritize funding for proposals that can move quickly, reduce project risk, and demonstrate local support and/or regional cooperation. It states that states and localities can show this commitment through:

* Expedited processes for environmental, health and safety reviews and permits.
* Liaisons to assist with site selection, supplier discovery, and compliance with local laws.
* A systems integrator that works with ecosystem companies to address shared issues like navigating permits, building infrastructure, finding workers, and coordinating incentive applications.
* Planning and support for other ancillary investments such as housing and community development.
* Where relevant, partnership with other states and localities to develop regional ecosystems and corridors that encompass multiple jurisdictions.[[7]](#footnote-7)

**The Path Forward for California**

California has the opportunity to capture a significant share of CHIPS Act funding, but competition will be intense and other states (Texas, New York, Arizona, Oregon and Ohio among others) are already shaping their own initiatives. Succeeding at a level that meets the state’s potential will require a strategy, a proactive outreach, and a well-organized partnership between the state, local governments, the business and economic development community, universities (including the University of California, CSU, and community colleges), and workforce development agencies.

This imperative is clear from the priority placed by the Department of Commerce, referenced above, on proposals that can move quickly and benefit from integrated public-private strategies that reduce cost and risk and expedite planning and delivery. This is a particular challenge for California, which is a high-cost state with regulatory processes such as CEQA often delay projects, adding to their cost and risk. Because of this it is important that California strategically prioritize the projects it chooses to pursue, develop a public-private framework for pursuing them, and be prepared to address workforce and regulatory barriers that reduce its competitiveness.

*Key Elements of a Strategy*

California for many purposes is uncompetitive on cost but can compete on value.

* **Fabs**: California can choose to go for large fabs, but due to cost and regulatory factors and the statutory and policy changes needed to address them the state may not be able to move with enough speed and clarity to compete with lower cost states with fewer legal and regulatory barriers. The well-known threat of CEQA litigation, for example, risks substantial permitting delays. Several elements are ultimately necessary to secure a fab: large shovel-ready tracts of land with entitlements for fab production, adjacent shovel-ready land for suppliers, a reliable supply of water, reliable and competitively priced electricity, a favorable tax and regulatory environment, and a strong pool of skilled and semi-skilled talent. Seismic risk is another factor that in California could affect site selection. No one element by itself is sufficient. In the aggregate, these requirements make competing for large fabs difficult almost everywhere in California. The strongest opportunity for large fabs in California is in the Central Valley, where land and housing costs are lower.

California may be more competitive, however, for smaller scale fabs (250-300 thousand square feet) and research laboratories whose construction and development entail lower cost and complexity. Small fabs and supply chain producers could locate in the Central Valley or in coastal regions.

* **Supply Chain:** California can also be competitive in attracting key parts of the manufacturing supply chain, where it is already strong. This can happen in existing technology centers where research is currently concentrated but is also an opportunity for inland areas where land is readily available, housing and other costs are lower, and economic development needs are greatest. Microelectronics should be a major focus. As with fabs, success in attracting supply chain investment to the Central Valley will require a strong workforce development and training component.
* **Research:** The University of California Council of Vice Chancellors of Research, which includes the ten UC campuses and the three UC-operated Department of Energy Labs Lawrence Berkeley National Laboratory, Lawrence Livermore National Laboratory and Los Alamos National Laboratory, is discussing microelectronics opportunities stemming from the CHIPS Act.

Multiple lab-university and lab-industry discussions are also underway. Participants in these discussions believe that California can play to several strengths including 1) workforce training at all levels (certificate, community college, university, graduate and post-graduate), 2) specialty applications and processes (e.g., harsh environments including space and environmental sensing, and optoelectronics, and 3) robust R&D programs at California’s universities, federal labs, and companies.

Bridging supply chain and applied research opportunities, California could focus on key innovations that require cooperation and optimization across the computing stack (where California is home to every industry segment) such as memory, logic, analog or specialty technologies. In building consortia, the historical U.S. experience with SEMATECH can provide a model.

*Playing to Strengths*

Across the state, project priorities should leverage areas where California enjoys a competitive advantage: semiconductor design and equipment manufacturing, R&D, innovation, strong research universities and national laboratories, and the largest and most highly skilled semiconductor workforce in the nation. With that, California has the best and deepest top-to-bottom semiconductor industry research and business infrastructure in the country with all sectors of the industry represented and is home to many of the nation’s leading companies:

* Intel, Qualcomm, Nvidia, Broadcom, AMD and Marvell are based in California
* Other industry leaders including Samsung, Texas Instruments, ARM and TSMC have a presence.
* Synopsis, Cadence Design Systems and Mentor Graphics - lead the world in design automation.
* California is also home to world leaders in manufacturing technology and solutions including KLA-Tencor, Lam Research, Applied Materials, and ASML.
* Leading electronic system companies that produce everything from smartphones to networking equipment and data centers – such as Apple, Alphabet, Microsoft, Meta, Amazon, Cisco and Tesla - have in-house chip design capabilities in California.
* California is home to two of the leading light sources (SLAC at Stanford and Berkeley Lab’s Advanced Light Source (ALS) that explore the time, energy and length dimensions of advanced semiconductor materials. Other advanced research in materials, electronic systems and computing architecture takes place at supercomputers at National Energy Research Supercomputing Center at Berkeley Lab) and the High-Performance Computing Innovation Center at (Lawrence Livermore National Laboratory.
* World-class prototyping facilities in California include the Marvell Nanofabrication Laboratory at UC Berkeley, the Stanford Nanofabrication Facility, and Nanofab at UC Santa Barbara and UCLA.
* The semiconductor California ecosystem, which leads on innovation, boasts large numbers of semiconductor startups and entrepreneurship programs such as Activate at Lawrence Berkeley National Laboratory’s Cyclotron Road. The state is home to the only incubator in the world focused on early-stage semiconductor startups – Silicon Catalyst.

As the heart of the nation’s venture capital industry, California is home to risk capital and venture finance companies such as Silicon Valley Bank with a significant focus on semiconductors at all stages.

This means that unlike in other states a strong ecosystem is in already place and doesn’t need to be created. The supporting economic and policy infrastructure for the industry in California, however, is weak. This is the gap that a state-led initiative needs to fill.

*Key Elements*

* **Workforce**: Integration of workforce training programs in the strategy is essential, drawing on existing manufacturing workforce training programs that can be directed to focus on semiconductor manufacturing skills as well as private sector programs. STEM skills, such as the ability to manage software and to work with machines, are increasingly important for modern manufacturing and should be a particular focus. This includes upskill training. Engaging disadvantaged communities in these programs will be essential, as well as mechanisms to facilitate small business participation. Community colleges must play a central role. Existing programs can be rapidly scaled. As one example, a partnership between SEMI, the industry association representing the electronics manufacturing and design supply chain, and Ignited Education, Foothill College, and the Krause Center for Innovation, has been awarded a $1 million California Apprenticeship Initiative New and Innovative Grant for the development of a semiconductor pre-apprenticeship and apprenticeship program to expand pathways to careers in the microelectronics industry.
* **Regional and Subregional Asset and Gap Analysis**: California’s manufacturing assets and gaps should be mapped regionally and sub-regionally to identify strengths as well as gaps where policy or other intervention is needed.
* **Cross-Regional Partnerships**: Federal criteria for CHIPS awards suggest that favorable consideration will be given to projects that are regional in nature and span multiple jurisdictions. In California this can happen through coastal-inland coalitions that leverage coastal advantages in R&D, IP and human capital with the cheaper land and lower labor costs available in the state’s interior. Possibilities include San Diego-Imperial County, Los Angeles-Inland Empire, and Bay Area-Sacramento-San Joaquin Valley. Whether inland or on the coast, Opportunity Zones should be considered in site selection.
* **A clearinghouse to expedite regulatory approvals and remove bottlenecks**: While state-led, this should include a structured public-private partnership that leverages the state’s policy resources with the on-the-ground capabilities and expertise in the business, economic development and educational sectors. That should include a quick response team (strike team) to address immediate opportunities and issues. Participants should include officials representing the Governor’s office and key state agencies, business and economic development organizations representing California and its regions, and prominent academics.
* **Federal and State Leadership Alignment**: Competing states’ Congressional delegations are engaging with leaders at the state and local level to support their CHIPS Act efforts. This happens, for example, through staff provided by Congressional leaders to lend insights and expertise to help state and local officials and their partners navigate the federal bureaucracy. A unified and engaged California’s Congressional delegation will increase the chances of success.

Examples of current California initiatives that coordinate and leverage activity across the state include the Climate Innovation Program, which directs funding for R&D grants to companies in California, and the ARCHES Hydrogen Hub initiative, which coordinates statewide activity focused on federal funding for hydrogen energy deployment.

*Policy Reforms and Initiatives*:

Regulatory changes may be needed to make California competitive for much of this investment, particularly as it relates to manufacturing. Large and small companies will compete on the merits for funding. The critical role of the state will be to show that if an applicant succeeds state programs to support their activity are available and can be included in their project proposal.

Because CHIPS funding is available now and major reforms will take time, the immediate focus should be on actions that can be delivered in a short period time. In the current economic environment steps that carve out the semiconductor sector will have a limited fiscal impact and may therefore be more achievable than broader reforms. As manufacturing in California is a priority across all sectors, longer term reforms should also be on the table.

Immediate initiatives should include:

* **Elimination of sales tax on the purchase of semiconductor manufacturing equipment, to both enable production at scale and support emerging companies that need equipment to design and test their products.**
* **To keep research and manufacturing in California, tax rebates on headcount as semiconductor startups hire.**

Other targets, connected to economic development in the state more generally, should include:

* **Wireless supply chain innovation**: The CHIPS+Science Act includes $1.5 billion for promoting and deploying wireless technologies that use open radio access networks (ORAN). Open source interfaces that are standardized and interoperable can support the diverse California companies that build the specialized hardware and software used in broadband networks, reducing supply chain risks. The state can assist the rollout of “lead-ahead” advancements by reducing barriers to infrastructure buildout and unnecessary delays in siting and permitting The Public Utilities Commission should also consider raising the technical assistance grant cap for local projects.
* **California Competes Act**: Tax credits available through the California Competes Act for companies choosing to locate and grow their businesses in California should be leveraged. $120 million is carved out in California Competes funding to support semiconductor investment.
* **Employment Training Panel:** The ETP should be customized to address the specific needs of the semiconductor industry. The ETP program cap should also be lifted to enable the participation of more mid-sized companies, and other steps taken to improve the cumbersome application and program set-up process.
* **Community Colleges**: introduce a semiconductor training module into community college curricula in regions where semiconductor activity is concentrated.
* **University of California/California State University Centers of Excellence**: The state should consider allocating resources to the UC and CSU systems for a semiconductor center or centers of excellence, with matching funds provided to help anchor federal grants and opportunities for applied research centers described in the Act (e.g., NSTC, Applied Packaging, etc.). The centers would leverage the UC system’s strong base in industry-university collaborative applied research and the CSU’s strength as the country’s largest producer of bachelor’s degrees.
* **Power and Water**: Semiconductor facilities, whether large fabs, small fabs, labs, or R&D, require significant power and water. Subsidies to build specialized infrastructure and/or to reduce utility costs may be needed to make California more competitive for semiconductor manufacturing.
* **Regional Technology Hubs**: securing sites in California for regional technology hubs, which can focus on semiconductors or other technologies, offers a signature opportunity. Hubs were not part of the CHIPS+Science Act appropriation but are expected to be funded in early 2023 and some funding is already being allocated from existing sources. Success in California will require highly focused public-private partnerships and strategic coordination by Go-Biz.

*Goals and Organization*

California’s effort to attract resources under the Act will run counter to pressure at the Federal level to direct investment toward the country’s interior and away from more prosperous coastal centers. This suggests a strategy where the Central Valley and inland California – which face many of the same economic and equity challenges seen elsewhere in the U.S. – play a key role.

California can also play to its strength in research, the depth of its semiconductor workforce, its innovative capacity, and its productivity in translating research and technological advances into products and applications – a key to future U.S. leadership in the sector. As a metric for the share of CHIPS investment the state should seek to secure, California’s share of the national semiconductor workforce (23%) might be a good target.

Leading states’ Congressional delegations are engaged with leaders at the state and local level to support their CHIPS Act efforts. The commitment from Congressional leaders includes staff that provide insights and expertise to help navigate opportunities in the federal bureaucracy. California’s Congressional delegation, 10% of the total membership of Congress, if unified, would have a disproportionate impact on the ability navigate and secure resources.

*How it Can Happen*

As an example of how resources can be aggregated to make regions in the state more competitive, the Greater Sacramento region is already growing its semiconductor manufacturing sector. In September 2022 Soladigm, the U.S. subsidiary of SK Hynix, the world’s second largest memory chip maker, announced plans to build its global research and development campus in Rancho Cordova. More than $100 million will be invested in the facility, which will be home to high-wage jobs and more than 1900 professionals. Proximity to a skilled workforce and the ability to expand to accommodate future growth were site selection factors, as was the availability of low-cost, high-uptime power, which was secured with the cooperation of the Sacramento Municipal Utility District (SMUD).

Elsewhere in the Greater Sacramento region the University of California at Davis, and looking to opportunities afforded by the CHIPS Act, is developing a focus on workforce development in rural and underserved communities, recognizing the priority this will receive at the federal level and at the National Science Foundation’s new directorate for translational research created by the CHIPS+Science Act. Resources will be focused on the development of its new Aggie Square district in Sacramento as a platform for translational research, including industry collaboration and support for startups. The university has also invested $22 million in in CHM2, a new clean room facility developed in partnership with Lawrence Berkeley National Laboratory and CITRIS (the Center for Information Technology Research in Service to Society), which leverages capabilities at four Northern California UC campuses – Davis, Berkeley, Merced and Santa Cruz. The clean room is accessible to industry and particularly enables prototyping.

The strategy leverages a workforce initiative at CITRIS that specifically includes a semiconductor component. At the K-12 level this incorporates connections to school districts in Davis, Sacramento and Stockton, providing mentorship and the opportunity to work in the CH2M clean room. That in turn is designed to expose high school students to the microelectronics sector and help to build a long-term workforce pipeline by preparing them for study in the microelectronics department at Davis. Partners include Sacramento City College, which is part of the California Community College system.

Similar assets are available in Southern California. UC San Diego has invested heavily in a state-of-the-art nanofabrication clean room facility, developed as part of the San Diego Nanotechnology Infrastructure (SDNI) initiative, which is one of 16 nationwide sites of the NSF-supported National Nanotechnology Coordinated Infrastructure (NNCI) program. The nanofabrication facility is also a part of the California Institute for Telecommunications and Information Technology (CALIT2), which leverages the capabilities at three Southern California UC campuses – San Diego, Irvine, and Riverside. Like CITRIS, CalIT2 partners closely with industry. The SDNI facility already plays a role in California’s innovation ecosystem, in part through workforce training in semiconductors. UC San Diego and SDNI have developed Integrated Circuit Education Kits to support workforce development at the college level, dozens of high school science teachers participate in enrichment summer camps each year, and over a thousand high school students are offered the opportunity to gain hands-on experience working with nanotechnologies on campus.

1. White House Fact Sheet, “CHIPS and Science Act Will Lower Costs, Create Jobs, Strengthen Supply Chains, and Counter China”, August 9, 2022. [↑](#footnote-ref-1)
2. Omar Villafranca, “Chip Shortage Cost U.S. economy billions in 2021”, CBS News, January 28, 2022. [↑](#footnote-ref-2)
3. Semiconductor Industry Association and Oxford Economics, “Chipping In: The Positive Impact of the Semiconductor Industry on the American Workforce and How Federal Industry Incentives Will Increase Domestic Jobs”, May 2021. [↑](#footnote-ref-3)
4. Asa Fitch and Dean Seal, “Micron to Build Biggest U.S. Chip Factory”, Wall Street Journal, October 5, 2022. [↑](#footnote-ref-4)
5. Reuters, “Qualcomm to Spend $4.8 Billion More on Chips from GlobalFoundries”, August 8, 2022. <https://www.reuters.com/technology/qualcomm-globalfoundries-sign-pact-doube-chip-manufacturing-2022-08-08>. [↑](#footnote-ref-5)
6. Mark Williams, “Here’s How Ohio Won a Bid by Intel to Build the World’s Largest Chip Factory in Ohio”, The Columbus Dispatch, January 21, 2022. [↑](#footnote-ref-6)
7. For more detail on investment goals and criteria see U.S. Department of Commerce, “CHIPS for America: A Strategy for the CHIPS for America Fund”, September 6, 2022. <https://www.CHIPS.gov>. [↑](#footnote-ref-7)